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10/784,134	02/20/2004	Gerd Frankowsky	INF 2233-US	5383

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EXAMINER

SIDDIQUI, SAQIB JAVAID

ART UNIT PAPER NUMBER

2138

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/784,134	Applicant(s) FRANKOWSKY, GERD	
	Examiner Saqib J. Siddiqui	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 2, 3, 13 and 21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4-12 and 14-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicant's response was received and entered November 13, 2006.

- Claims 1 & 4-21 are pending. Claims 1, 4, 7, 15 & 18 are amended.
- Claims 2-3, 13 & 21 are canceled.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1 & 4-21 filed November 13, 2006 have been fully considered but they are not persuasive.

Applicant contends that the prior art of record Arase US Pat no. 5,808,945 fails to teach or suggest the limitation "if defective memory areas that are addressable by a common word line group exceeds a first maximum number." Further, Applicant explains that the comparison is a quantitative comparison and not a numeric comparison. Examiner accepts Applicants contention but would like to respectfully explain that the limitation argued by the Applicant has been canceled and the new limitation reads: "word line groups of the memory module that are forced to be replaced because each one addresses a number of defective memory areas that is greater than a first maximum number." Here there is no mention of a comparison and given the broadest possible interpretation of the claims Arase teaches replacing word line groups which represent a number of defective memory areas (the address represents a number of

defective areas) that is greater than a first maximum number (again an address numerically represented).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., number of defective memory areas exceeds a maximum number) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4-5, 7-10, & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Namekawa US Pat no. US 6115301 A and further in view of Arase US 5808945 A

As per claim 1:

Namekawa substantially teaches a method for determining a repair solution for a memory module in a test system (Figure 1, column 3, lines 20-65), comprising: determining, for each memory area of the memory module, a defect datum (column 7, lines 1-45); generating defect addresses for all defective memory areas (column 7, lines 20-55); storing the defect addresses in the test system (Figure 2 # 80, column 6, lines 30-65); identifying a set of available redundant word line groups and bit line groups (column 7, lines 35-50), wherein each memory area is addressable via a word line group comprising one or more word lines (column 5, "WL") or via a bit line group comprising one or more bit lines (column 5, "BL"); and determining the repair solution for remaining defective memory areas from the set of available redundant line groups (Figure 1, columns 3-4, lines 45-36).

Namekawa does not explicitly teach the method of claim 1, wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number.

However, Arase in an analogous art teaches the method wherein of identifying and replacing the one or more defective word line groups with respect to first maximum number (Figure 1, columns 3-4, lines 45-36) and identifying and replacing the one or more defective word line groups with respect to first maximum number (Figure 3, column 5, lines 10-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to replace the defective memory using redundant bit line or word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence replacing them with respect to configurations is a different yet obvious criteria of replacement. Further it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 4:

Namekawa/Arase teach the method as rejected in claim 1, wherein the first maximum number corresponds to available redundant bit line groups (Arase, Figure 3, column 5, lines 20-45) and the second maximum number corresponds to available redundant word line groups (Arase, Figure 4, column 5, lines 55-67).

As per claim 5:

Namekawa substantially teaches a method as rejected in claim 1 above, wherein defect addresses are stored in a memory unit which includes a second memory

segment having a second number of defect address memory locations for storing defect addresses in a bit line group (column 6, lines 50-65).

Namekawa does not explicitly teach a first memory segment having a second number of defect address memory locations for storing defect addresses in a word line group.

However Arase in an analogous art teaches a first memory segment having a second number of defect address memory locations for storing defect addresses in a word line group (Figure 1, columns 3-4, lines 45-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to store the defective address using word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence storing them with respect to configurations is a different yet obvious criteria of storing. Further it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 7:

Namekawa substantially teaches a test device for determining a repair solution for a memory module (Figure 1, column 3, lines 20-65), comprising: a control unit for carrying out a test operation for memory areas in the memory module and determining defective memory areas (column 7, lines 1-45); a memory unit for storing defect addresses of defective memory areas (Figure 2 # 80, column 6, lines 30-65); a

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converter circuit for converting defect data corresponding to defect memory areas into defect addresses for storing in the memory unit (column 7, lines 20-55); and an evaluation unit for selecting one or more replacement redundant groups based on the stored defect addresses (column 7, lines 35-50, see rejections under claim 1 above).

Namekawa does not explicitly teach the method of claim 1, wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number.

However Arase in an analogous art teaches the method wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number (Figure 1, columns 3-4, lines 45-56) and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number (Figure 3, column 5, lines 10-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to replace the defective memory using redundant bit line or word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence replacing them with respect to configurations is a different yet obvious criteria of replacement. Further it has been held that where general

conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 8:

Namekawa teaches the test device as rejected in claim 7 above.

Namekawa does not teach an evaluation unit, which selects the one or more replacement redundant groups from one or more redundant word line groups and one or more redundant bit line groups.

However Arase in an analogous art teaches the method wherein the one or more replacement redundant groups are selected from a redundant word line groups (Figure 1, columns 3-4, lines 45-36) and from a redundant bit line group (Figure 3, column 5, lines 10-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to replace the defective memory using redundant bit line or word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence replacing them with respect to configurations is a different yet obvious criteria of replacement. Further it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 9:

Namekawa/Arase substantially teaches the test device as rejected in claim 8 above, wherein a second memory segment having a second number of defect address

memory locations for storing defect addresses in a bit line group (column 6, lines 50-65).

Namekawa does not explicitly teach a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group.

However Arase in an analogous art teaches a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group (Figure 1, columns 3-4, lines 45-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to store the defective address using word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence storing them with respect to configurations is a different yet obvious criteria of storing. Further it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 10:

Namekawa/Arase teach the test device as rejected in claim 9, wherein the first number corresponds to available redundant bit line groups (Arase, Figure 3, column 5, lines 20-45) and the second number corresponds to available redundant word line groups (Arase, Figure 4, column 5, lines 55-67) on the memory module.

As per claim 15:

Namekawa substantially teaches a test system, comprising: a connectable memory module (column 7, lines 1-45); and a test device, connectable to the memory module, for determining a repair solution for the memory module (Figure 1, column 3, lines 20-65), the test device comprising a control unit for carrying out a test operation for memory areas in the memory module and determining defective memory areas (column 7, lines 20-55), a memory unit for storing defect addresses of defective memory areas (Figure 2 # 80, column 6, lines 30-65), and an evaluation unit for selecting one or more replacement redundant groups based on the stored defect addresses (column 7, lines 35-50, see rejections under claim 1 above).

Namekawa does not explicitly teach the method of claim 1, wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number.

However Arase in an analogous art teaches the method wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number (Figure 1, columns 3-4, lines 45-56) and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number (Figure 3, column 5, lines 10-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

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enable Namekawa's invention to be able to replace the defective memory using redundant bit line or word line groups, because one of ordinary skill in the art would have realized that the memory cells in Namekawa's invention are already configured in terms of word and bit lines, hence replacing them with respect to configurations is a different yet obvious criteria of replacement. Further it has been held that where general conditions of a claim are disclosed in the prior art, discovering the optimum or **workable** ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Claims 6, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Namekawa US Pat no. US 6115301 A in view of Arase US 5808945 A, and further in view of Bemis US Pat no. 4692894 A.

As per claim 6:

Namekawa/Arase teach the method as rejected in claim 5, wherein the evaluation unit unconditionally defines a redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group (Figure 1, columns 3-4, lines 45-36), and unconditionally defining a redundant bit line group as repair solution for the defective memory areas which can be addressed via a bit line group (Figure 3, column 5, lines 10-65).

Namekawa/Arase does not explicitly teach an overflow register.

However, Bemis in an analogous art teaches a memory array with an overflow register that detects overflow (Abstract lines 3-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's

invention to be able to detect overflow, because one of ordinary skill in the art would have realized that including an overflow register would have prevented data loss.

As per claim 11:

Namekawa/Arase teach the test device as rejected in claim 9.

Namekawa/Arase does not explicitly teach an overflow register.

However, Bemis in an analogous art teaches a memory array with an overflow register that detects overflow (Abstract lines 3-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to be able to detect overflow, because one of ordinary skill in the art would have realized that including an overflow register would have prevented data loss.

As per claim 12:

Namekawa/Arase teach the test device as rejected in claim 11, wherein the evaluation unit unconditionally defines a redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group (Figure 1, columns 3-4, lines 45-36), and unconditionally defining a redundant bit line group as repair solution for the defective memory areas which can be addressed via a bit line group (Figure 3, column 5, lines 10-65).

Namekawa/Arase does not explicitly teach an overflow register.

However, Bemis in an analogous art teaches a memory array with an overflow register that detects overflow (Abstract lines 3-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's

invention to be able to detect overflow, because one of ordinary skill in the art would have realized that including an overflow register would have prevented data loss.

Claims 14, 16, & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Namekawa/Arase in view of Sakata US PG-Pub no. 20010045581 A1.

As per claim 14:

Namekawa/Arase teaches the test device as rejected in claim 7.

Namekawa/Arase does not teach a test device further comprising a comparison circuit.

However, Sakata in an analogous art teaches a test device further comprising: a comparator circuit for comparing written data and read-out data to generate defect data (Figure 2, paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to compare written data and read out data, since doing so would have allowed for a better analysis of the defect data.

As per claims 16 & 17:

Namekawa teaches a test system as rejected in claim 15.

Namekawa does not teach a test device further comprising a comparison circuit.

However, Sakata in an analogous art teaches a test device further comprising: a comparator circuit for comparing written data and read-out data to generate defect data (Figure 2, paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Namekawa's invention to compare

written data and read out data, since doing so would have allowed for a better analysis of the defect data.

As per claims 18-20:

Claims 18-20 are directed to a method of the test system and method of Claims 1-17. Namekawa, Arase, Bemis, and Sakata alone or in combination as stated above, the system and method as set forth in Claims 1-17. Therefore, Namekawa, Arase, Bemis, and Sakata also teach, either alone or in combination as stated above, the method as set forth in Claims 18-20.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US PG Pub no. (20030009615 A1, 20010045581 A1, 20010026486 A1) and US Pat no. (6236615 B1, 5798974 A 6367030 B1) mention the same redundant testing system using the defective address as the criteria for replacement.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

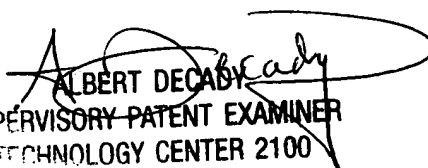
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2138
12/01/2006


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